

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-25 (cancelled)

1        26. (original) A semiconductor apparatus comprising:  
2        a nonvolatile memory; and  
3        a central processing unit,

4        wherein said nonvolatile memory has a plurality of  
5 memory cells,

6        wherein each of said memory cells includes:

7            a memory gate formed over a first semiconductor  
8 region with a first insulating film and a second insulating  
9 film interposed therebetween;

10           a first switch gate formed over said first  
11 semiconductor region to a first side of said memory gate  
12 with a third insulating film;

13           a second switch gate formed over the first  
14 semiconductor region to a second side of said memory gate  
15 with a fourth insulating film, wherein said second side is  
16 opposite said first side across said memory gate; and

17           a second semiconductor region and a third  
18 semiconductor region respectively formed adjacent to  
19 opposite sides of said first semiconductor region; and

20            wherein said first nonvolatile memory is capable of  
21 storing a program and data, and  
22            wherein said central processing unit executes said  
23 program read from said first nonvolatile memory.

1            27. (original) A semiconductor apparatus according  
2 to claim 26, further comprising a random access memory,  
3            wherein said random access memory is used for a work  
4 memory for said central processing unit.

1            28. (original) A semiconductor apparatus according  
2 to claim 27,  
3            wherein said central processing unit controls to  
4 access to said nonvolatile memory.

1            29. (original) A semiconductor apparatus according  
2 to claim 28, wherein said nonvolatile memory is capable of  
3 rewriting data stored therein.

1            30. (original) A semiconductor apparatus according  
2 to claim 29, further comprising a second nonvolatile  
3 memory,

4        wherein said central processing unit controls to  
5        access to said second nonvolatile memory.

1        31. (original) A semiconductor apparatus according  
2        to claim 29, further comprising a communication circuit and  
3        an antenna,

4        wherein said communication circuit couples to said  
5        antenna, and

6        wherein said communication circuit is capable of  
7        communication by electromagnetic induction.

1        32. (original) A semiconductor apparatus according  
2        to claim 26,

3        wherein each said memory cell is capable of storing  
4        data by trapping electrons in said memory gate thereof to  
5        change a threshold voltage.